REMARKS/ARGUMENTS

Claims 1-20 are pending in the present application. Reconsideration of the claims is respectfully requested. Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification.

I Interview Summary

Applicants thank Examiner Ilwoo Park for the courtesies extended to Applicants' representatives during the April 18, 2006 telephone interview. During the interview, Applicants' representatives discussed the distinction between the claims and the *Browen* reference. The Examiner agreed with the distinctions drawn by the Applicants between *Browen* and features of claim 1 and indicated that the rejection of the claims based on this reference were overcome. The Examiner said that he would issue a second non-final office action upon the receipt of the present response. No agreement was reached as to other rejections under 35 U.S.C. §§ 101, 112, and 103.

II 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 7 and 15 under 35 U.S.C. § 112, second paragraph, as being indefinite. This rejection is respectfully traversed.

The Examiner has rejected these claims stating:

> 6. Claims 7 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Office Action dated March 1, 2006, p. 4.

Claim 7 is representative of all claims in this group and recites:

> 7. The method of claim 6, wherein the step of setting the length comprises:
> setting the length field as follows:
> length field = (ABS(frame size/CLS)+1)*CLS,
> wherein CLS is the cache length size.

Applicants respectfully point out that the letters ABS when used in the form shown in claims 7 and 15, in a mathematical expression as shown, stand for the mathematical function "Absolute Number." The mathematical function ABS returns the absolute value of its numerical parameters, a number without a sign. This function is commonly taught as a part of high school mathematics curricula and extensively used in programming languages to denote the mathematical function |x|. See, http://www.analyzemath.com/Definition-Absolute-Value/Definition-Absolute-Value.html;

http://www.w3schools.com/wmlscript/lang_abs.asp. Detailed texts of these sources are included in Appendices A and B respectively.

Applicants do not claim the mathematical function ABS as their invention in claims 7 and 15. The Applicants only rely on this commonly used mathematical function to claim the unique features of claims 7 and 15 that depend upon or use the mathematical function ABS. Therefore, the applicants respectfully request that the rejection of claims 7 and 15 under 35 U.S.C. § 112, second paragraph should be withdrawn.

III 35 U.S.C. § 101

The Examiner has rejected claims 17-18 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter.

The Examiner has rejected these claims stating:

> • Claims 17 and 18 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The present claims recite "a computer program product in a computer readable medium". This medium is not recited as "storage" or "tangible" and therefore does not fall within the categories of patentable subject matter (e.g. process, machine, manufacture, or composition of matter, or any new and useful improvement thereof).
> • Claims 17 and 18 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. These claims recite instructions for performing particular functions (e.g. "receiving" and "setting"). However, these instructions lack practical application.

Office Action dated March 1, 2006, pp. 4-5.

Section 101 of Title 35 U.S.C. sets forth the subject matter that can be patented:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.

"[N]o patent is available for a discovery, however useful, novel, and nonobvious, unless it falls within one of the express categories of patentable subject matter of 35 U.S.C. § 101." Kewanee Oil Co. v. Bicron *Corp.*, 416 U.S. 470, 483, 181 USPQ 673,679 (1974). The statutory categories of § 101 define eligible (patentable or statutory) subject matter, i.e., subject matter that can be patented. The listed statutory categories of invention are "process, machine, manufacture, or composition of matter."

Claim 17 is representative of all claims in this group and recites:

> 17. A computer program product in a computer readable medium for transferring data from a memory to a network adapter, the computer program product comprising:
>
> first instructions for receiving a request to transfer data in the memory to a network adapter;
>
> second instructions for setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size.

In the present case, claim 17 clearly and unquestionably recites a "product," an article of manufacture, embodied in a tangible computer usable medium, implementing the method of claim 1. Section 100(b) of Title 35 U.S.C. defines "process" to mean, "process, art or method, and includes a new use of a known process, machine, manufacture, composition of matter, or material." The definition of "process" to mean "process, art or method" makes it clear that the terms are synonymous. *See*, S. Rep. No. 1979, reprinted in 1952 U.S. Code Cong. & Admin. News at 2409-10. The Office cannot creatively redefine the claimed invention to be something other than what is explicitly recited in the claim for the sole purpose of rejecting the claim, and in this case, claim 1 recites a method. Therefore, the invention of claim 1 falls within the statutory categories of patentable subject matter because the claim recites a method. Therefore, claim 17 which claims a product implementing the method of claim 1 is also directed to statutory subject matter under 35 U.S.C. § 101.

Furthermore, the invention of claim 17 produces useful and tangible results with well-known practical applications in the pertinent industry. Claim 17 recites "second instructions for setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size." A data transfer from computer memory to input/output sub-systems is more efficient when the data being transferred is cache aligned.

> With respect to transferring data between a memory subsystem and an input/output (I/O) subsystem using a PCI bus, efficiencies in transferring data are dependent on cache aligned data transfers from the memory subsystem to the I/O subsystem. Efficiencies are greatest when the total data transfer is an integral multiple of the cache line size (CLS). For example, transfers to a disk storage system fit this model in which typical transfers have sizes, such as 512, 1024, 2048, and 4096 bytes.
>
> ...
>
> These efficiencies are typically not found with some I/O subsystems, such as network adapters. If the data in memory is cache aligned, the data may be read from prefetch memory **410**. The present invention adds additional dummy data to allow for cache alignment. As a result, DMA transfers of data from the system memory to the network adapter may be made more efficiently as described

> below. Further, this additional data is discarded by the network adapter when data is transferred by the network adapter.

Specification, p. 2, ll. 3-13; p. 13, ll. 21-28.

A method or product that improves data transfer efficiency, by the very description exudes utility, benefit, and distinct advantages in the computer hardware and software industry. Higher efficiency of data transfer implies more data transferred over an existing bandwidth, same data transfer over a smaller bandwidth, or both. In each case, the method or product so affecting data transfer directly implicates fiscal benefits, performance benefits, or ease of implementation. In each case, the advantages of the method or product are discretely quantifiable, and therefore of patentable utility. Therefore, the invention of claim 17, which teaches a more efficient way of transferring data, produces a useful result, has practical applications, and therefore comprises patentable subject matter.

Furthermore, the invention of claim 17 is patentable in view of new guidelines covering patentability of claims directed to a process in a computer readable medium. The USPTO Guideline for evaluating computer-readable medium encoded with functional descriptive material, such as a computer program, expressly states that a claim to such computer-readable medium when so encoded is statutory subject matter. USPTO, *Interim Guideline for Examination of Patent Application for Patent Subject Matter Eligibility* (26 Oct. 2005) (hereinafter "Guideline"). The Guideline provides, in relevant part:

> "[A] claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory."

Id., p. 52.

The Guideline further provides:

> Claims that recite nothing but the physical characteristics of a form of energy, such as a frequency, voltage, or the strength of a magnetic field, define energy or magnetism, per se, and as such are nonstatutory natural phenomena. O'Reilly, 56 U.S. (15 How.) at 112-14. Moreover, it does not appear that a claim reciting a signal encoded with functional descriptive material falls within any of the categories of patentable subject matter set forth in § 101.
>
> ...
>
> These interim guidelines propose that such signal claims are ineligible for patent protection because they do not fall within any of the four statutory classes of § 101. Public comment is sought for further evaluation of this question.

Id., pp. 55-56.

Claim 17 is directed to a computer program product in a computer readable medium. As the Guideline provides, "a computer readable medium with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized" is statutory. Because claim 17 recites a computer

program product in a computer readable medium, along with the other recited steps, claim 17 does describe a data structure that defines structural and functional interrelationships between the data structure and the computer software and hardware components, which permit the data structure's functionality to be realized. Thus, claim 17 is patentable subject mater under 35 U.S.C. § 101, as explained under the Guideline.

The claim recites a "computer readable medium" in which a signal is embedded. Claim 17 claims functional descriptive material encoded on a computer readable medium and does not claim signals encoded with functional descriptive material. For this additional reason, claim 17 falls under allowable statutory matter under 35 U.S.C. § 101.

Claim 17 comprises statutory subject matter because the claim is directed towards the medium, and not to the radio frequency or the light wave signals that may inherently be used in such media technologies. The use of radio frequency or light wave as a method of encoding or recording the computer program onto such medium does not render the medium itself nonstatutory. Even in case of a CD-ROM, a laser form of light wave is used for accomplishing the encoding/recording of the information on to the CD-ROM, yet the CD-ROM remains a well-accepted computer readable medium. Encoding the air or glass fiber medium with radio frequency or light wave similarly cannot render the air or glass fiber medium nonstatutory under § 101.

Thus, based on the MPEP and applicable case law, claim 17 is statutory under 35 U.S.C. § 101. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 17-18 under 35 U.S.C. § 101.

IV 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-3, 5, 9-11, 13, 17 and 19 under 35 U.S.C. § 102(e) as being anticipated by *Browen*, PCI-X bus system testing and verification apparatus and method, United States Patent No. 6,633,832 B1 (issued, October 14, 2003), (hereinafter, "*Browen*"). This rejection is respectfully traversed.

The Examiner has rejected claim 1 stating:

> Regarding **claim 1**, Browen teaches a method for transferring data from a memory to a network adapter (see col. 3, lines 6-7 and 12-13) . The reference teaches receiving a request (see Figure 3; col. 4, line 29) to transfer data in the memory to a network adapter; and setting a transfer size to align the data (see col. 4, lines 37-40) with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size (see col. 4, lines 29-31).

Office Action dated March 1, 2006, p. 6.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case, each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Claim 1 recites:

> 1. (Original) A method in a data processing system for transferring data from a memory to a network adapter, the method comprising:
> receiving a request to transfer data in the memory to a network adapter; and
> setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size.

Contrary to the Examiner's assertion, *Browen* does not teach the setting step of the method of claim 1. Particularly, in the setting step, *Browen* does not teach the feature, "setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size." The Examiner cites the following section of *Browen* as teaching this feature:

> Also, the desired source/destination address alignment for the transaction is set. This allows for full testing on various memory address alignments and cache boundaries.

Browen, Col. 4, ll. 37-40.

Browen teaches a setting step that is not the same as the setting step as recited in claim 1. *Browen* teaches a method to test PCI-X devices for compliance with the PCI-X standard. In the process of this testing, *Browen's* setting step involves setting the source/destination address alignment so that the memory addresses accessed for the read/write can be tested for compliance with the cache boundaries. In contrast, claim 1 recites setting a transfer size to align data with a cache line size. Setting this transfer size in claim 1 is not the same as setting a source/destination address alignment in the cited reference.

In *Browen*, the purpose of this address alignment is described as follows:

> Possible data phase behaviors include masking byte enables at the beginning and end of a sequence and disconnecting at a specified ADB in the transaction.

Browen, col. 4, ll. 49-51.

Through this step, *Browen* seeks to test whether the transfer of data during the PCI-X testing occurs at the allowable disconnect boundaries, the boundaries being memory address boundaries. This step in *Browen* is distinct from the setting step as recited in claim 1. The step in claim 1 states "setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size," and "wherein an amount of data is less than or equal to the transfer size." The first of these two features of the setting step in claim 1 states that the transfer size is set to align with the cache line size, and not an address alignment with cache boundary as *Browen* teaches. As is well known in the art, a memory address is distinct from and not reflective of the memory size. Therefore, without more, memory address alignment alone does not teach memory size alignment. *Browen* discloses the former, the feature of claim 1 recites the latter, and therefore, the two are distinct from one another.

The setting step is dependent on a condition for determining when the setting of transfer size occurs. This condition, "if the amount of data to be transferred is unequal to the cache line size" is not taught by *Browen* in the entire disclosure. *Browen* does not teach this condition because *Browen* is not concerned with efficiency of the data transfer in cases where the transferred data is of a different size than the size of the memory cache. *Browen*, in general is directed towards PCI-X device testing for PCI-X protocol compliance, and not efficiency of data transfer. In the cited section in particular, *Browen* is concerned with testing for any violation of the memory address boundary conditions. The feature recited in claim 1, on the other hand, does not refer to memory addresses. In the section of *Browen*, that the Examiner seeks support from, any reference to size alignment that the feature of claim 1 states is notably absent. Also absent in *Browen* is the teaching of the condition when the size alignment occurs. Therefore, *Browen* does not teach, "setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size."

By the same reason as described above, *Browen* also does not teach, the second part of the setting step of claim 1, namely, "wherein an amount of data is less than or equal to the transfer size." Absent in the entire disclosure of *Browen* is any discussion of efficiently handling various sizes of data transfers. *Browen* therefore does not teach a further step where if an amount of data to be transferred is less than the transfer size, and the steps of making the transfer of such data efficient. Thus, *Browen* does not anticipate claim 1. For the same reasons, independent claims 9, 17, and 19 are also not anticipated by *Browen* because they contain features similar to those in claim 1. Further, dependent claims 2, 5, 10, and 13 are not anticipated by *Browen* because they depend from one of these independent claims. Thus, *Browen* does not anticipate claims 1-2, 5, 9-10, 13, 17, and 19 under 35 U.S.C. § 102(e).

Claim 3, which depends from claim 1, includes additional features not shown by *Browen*. The Examiner further rejects this claim on additional grounds, stating:

> As for **claim 3,** Browen teaches a length indicator is set to the amount of data and the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the network adapter (see col. 4, lines **52-56,** *PcI-X transaction is initiated with the programmed alignment and any relevant behavior properties).*

Office Action dated March 01, 2006, p. 6.

Claim 3 recites:

> 3. The method of claim 1, wherein a valid length indicator is set to the amount of data and wherein the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the network adapter.

The Examiner cites the following section from *Browen* in support of the rejection:

> In step 312 a PCI-X transaction is initiated, starting with the programmed source/destination address alignment as well as the selected PCI-X command and any relevant behavior properties specific to the Address/Command phase (i.e., 32-bit or 64-bit operation).

Browen, col. 4, ll. 52-56.

Contrary to the Examiner's assertion, *Browen* fails to teach the feature "valid length indicator" of claim 3. The Examiner relies on the statement "any relevant behavior properties" as teaching the valid length indicator as claimed, and construes *Browen's* teaching in a manner inconsistent with *Browen's* description. The Examiner's selection of the phrase – any relevant behavior properties – from *Browen's* disclosure is misleading because the Examiner has left out the qualifier to that phrase that properly defines the scope of the phrase in *Browen's* disclosure. *Browen* suggests "any relevant behavior properties specific to the Address/Command phase" and therefore must be construed with that specificity to be considered as taught by *Browen*. Without the limitation of that specificity, the phrase, as the Examiner has asserted against the claim, engulfs every property of every PCI or PCI-X device ever invented. Clearly, this assertion is not supported by *Browen*. *Browen* teaches the address/command phase behavior properties, examples of which are 32-bit or 64-bit operation, with respect to a PCI-X transaction configuration of a PCI-X requester. This teaching is limited to selecting the address/attribute phase behavior of the PCI requester during the testing. The phrase "any relevant behavior properties" therefore relates to selection of address/attribute phase and data phase behavior properties in *Browen's* PCI-X testing system, and not the valid length of the data a network adapter must put out from the transferred data that the adapter receives. Claim 1 recites a valid length indicator that is written by the network adapter device driver into the system memory and sent with the data stream to the network adapter. This valid length indicator is used for indicating to the network adapter the length of valid data in the transferred segment of data that the adapter must put out on the network. The definition, purpose,

and use of the valid length indicator in claim 3 are thus distinct from any property of the address/command phase contemplated by *Browen*.

Therefore, *Browen's* statement – any relevant behavior properties specific to address/command phase – does not anticipate a valid length indicator as described. Because *Browen* does not disclose "valid length indicator" feature of claim 3, *Browen* cannot anticipate claim 3 under 35 U.S.C. § 102(e). Because claim 11 contains features similar to those in claim 3, *Browen* does not anticipate claim 11 for the same reasons.

V 35 U.S.C. § 103, Obviousness

V.A As to Claims 4 and 12

The Examiner has rejected claims 4 and 12 under 35 U.S.C. § 103(a) as being unpatentable over *Browen*, in view of *McCrory* et al., System and Method for Software Controlled Cache Line Affinity Enhancements, United States Patent Application 2002/0095554 A1 (Published, July 18, 2002) (hereinafter, "*McCrory*"). This rejection is respectfully traversed.

The Examiner has rejected claim 4 stating:

> As for claim 4, Browen does not teach the cache line size, as being 2^n, where in n is a positive integer. As for this limitation, Mccrory et al. teaches cache line size as being a power of 2 (see 2^n) . The Mccrory et al. also teaches this size where n is a positive integer (see "16, 32, 64, 128", Page 3, paragraph 0036) . At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a method including a "typical" cache line size, as taught by McCrory et al. (see Id.)

Office Action dated March 1, 2006, p. 9.

Claim 4 is representative of all claims in this group and recites:

> 4. The method of claim 1, wherein the cache line size is 2^n, wherein n is a positive integer.

V.A.1 The Proposed Combination Does Not Teach all of the Features of Claim 4

The Examiner has failed to state a *prima facie* obviousness rejection because the proposed combination does not teach all of the features of claim 4. A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). In the case at hand, not all of the features of the claimed invention have been considered and the teachings of the references themselves do not suggest the claimed subject matter to a person of ordinary skill in the art.

Claim 4 claims a method depending from the method of claim 1. Therefore, the distinctions between *Browen* and claim 1 apply in the same manner to claim 4 so that *Browen* does not anticipate claim 4 either. Specifically, *Browen* does not teach the claim 1 feature "setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size."

The Examiner admits that *Browen* does not teach, "wherein the cache line size is 2^n, wherein n is a positive integer" feature of claim 4. The Examiner seeks to use *McCrory* to satisfy missing features in *Browen*. However, the combination of *Browen* and *McCrory* cannot teach all features of claim 1 because *McCrory* does not overcome the deficiencies in *Browen*. In the sections that the Examiner cites from McCrory, McCrory states:

> [0036] In an MP computer system, the memory addresses associated with each cache line are unique, and thus the common portion of the memory address range shared by each byte in the same cache line is referred to as the cache line tag. The cache line tag maps the cache to a location in main memory. Normally, the cache line size (in bytes) is a power of 2 (e.g. 16, 32, 64, 128, etc). Typically, a cache line is a set size of bytes for a particular MP computer system. For example, Intel Corporation's Pentium.RTM. Processor family utilizes 32 byte cache lines. Thus some lower bits within the memory address are used to distinguish a specific byte or beginning range of bytes within the cache line. These lower address bits are not considered part of the tag, since they are not common between all the bytes in the memory address range associated with the cache line.

McCrory, p. 3, para. 0036.

McCrory teaches improving multi-processor system performance by minimizing cache coherency operations through the use of cache line affinity bits to intelligently modify requests for cache lines. *McCrory* is concerned with avoiding unnecessary cache coherency operations when a caching agent requests broader cache permissions than are actually needed. Applicants have shown in section IV above, that *Browen* does not teach "setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size." Applicants have also shown in the same section that *Browen* does not teach, "wherein an amount of data is less than or equal to the transfer size." Nothing in *McCrory's* entire disclosure teaches or suggests these two features that are missing from *Browen*. Because *McCrory* is not concerned with making data transfer between a memory and a network adapter efficient, *McCrory* fails to disclose any mechanism to accomplish that function. As a result, *McCrory* does not disclose either of the two features that are deficient in *Browen* as to claim 1.

Therefore, the combination of *Browen* in view of *McCrory* cannot teach all features of claim 4. Consequently, *Browen* in view of *McCrory* does not make claims 4 and 12 obvious under 35 USC § 103(a).

V.A.ii No Teaching, Suggestion, or Motivation Exists to Combine the References

In addition, a *prima facie* obviousness rejection against features of claim 4, has not been made because no proper teaching or suggestion to combine the references exists in the references. A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). A proper *prima facie* case of obviousness cannot be established by combining the teachings of the prior art absent some teaching, incentive, or suggestion supporting the combination. *In re Napier*, 55 F.3d 610, 613, 34 U.S.P.Q.2d 1782, 1784 (Fed. Cir. 1995); *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d 1566, 1568 (Fed. Cir. 1990). No such teaching or suggestion is present in the cited references and the Examiner has not pointed out any teaching or suggestion that is based on the prior art.

The Examiner has failed to state a *prima facie* obviousness rejection against features of claim 4, because the Examiner has not stated a proper teaching, suggestion, or motivation to combine the references. Instead, the Examiner has only stated a proposed advantage to combining the references. However, an advantage is not necessarily a teaching, suggestion, or motivation. To constitute a proper teaching, suggestion, or motivation, the Examiner must establish that one of ordinary skill would both recognize the advantage and have a reason to implement the advantage. For example, a first reference may disclose the use of lasers to achieve nuclear fusion. A second reference may disclose that ultra-high power lasers deliver more energy. One of ordinary skill may recognize that an ultra-high power laser would be more useful to achieve nuclear fusion, though one of ordinary skill would be motivated to avoid combining the references because of the extreme expense of ultra-high power lasers. In this example, one of ordinary skill is motivated to avoid implementing the combination, even if he or she recognized the advantage, and so no teaching, suggestion, or motivation exists to combine the references.

In the case at hand, the Examiner has not provided a sufficient reason why one of ordinary skill would recognize the proposed advantage or have a reason to implement it. The Examiner states,

> At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a method including a "typical" cache line size, as taught by McCrory et al. (see Id.)

Office action dated March 1, 2006, p. 9.

However, the proposed motivation does not actually exist because making a cache of the size disclosed by *McCrory* does not cure any shortcoming in *Browen's* system for accomplishing *Browen's* purpose. Regardless of the size of the cache, *Browen* is simply concerned with whether boundary conditions are violated during a PCI-X transaction. The fact that *McCrory* can potentially impart a cache of the size 2 to the power of an integer makes no difference to *Browen*. No deficiency exists in *Browen* that can be cured by taking into account *McCrory's* cache size. *Browen* is concerned with thorough testing for PCI-X protocol violation including allowable disconnect boundaries in the memory and the

cache, not preventing unnecessary cache coherency operations over a processor bus. Furthermore, *Browen* provides a complete system and method for testing PCI-X devices for protocol violations, and is not deficient in supporting that function. Because *Browen* is not lacking in this capability, *Browen's* existing disclosure vitiates any putative need for *McCrory's* teachings. For these reasons, the Examiner's statement fails to provide a proper teaching, suggestion, or motivation to combine the references. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against claims 4 and 12.

V.A.iii **The Examiner Used Impermissible Hindsight When Fashioning the Rejection**

In addition, the Examiner has failed to state a *prima facie* obviousness rejection against claim 4, because the Examiner used impermissible hindsight when fashioning the rejection. Personal opinion cannot be substituted for what the prior art teaches because a *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993).

The Examiner believes,

> At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a method including a "typical" cache line size, as taught by McCrory et al. (see Id.)
> Office action dated March 1, 2006, p. 9.

However, a simple substitution as the Examiner suggests would not change anything in *Browen's* operations to give any advantage to *Browen's* system directly or indirectly, and therefore will not produce the system as claimed by Applicants. Furthermore, as described above, *Browen* has no need for changing cache requests to avoid unnecessary cache coherency operations, in order to test for PCI-X protocol violations. *McCrory* fails to provide a reason to replace cache size in *Browen's* system, in the manner claimed by the Examiner. Thus, none of the references teaches or suggests combining the references as posited by the Examiner, to achieve the results of the claimed method, and one of ordinary skill would have no reason to combine or otherwise modify the references.

Based on the plain disclosures in the references, the only suggestion to modify the references is found in Applicant's specification. Hence, the Examiner must have used Applicant's specification to find a teaching, suggestion, or motivation to combine the references. Doing so is impermissible hindsight and fails to comport with the standards of *Graham v. John Deere Co.*, 383 U.S. 1 (1966), which requires a proper teaching, suggestion, or motivation to combine or modify references to achieve a proper obviousness rejection. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against claims 4 and 12.

V.A.iv **References Would Not Be Combined By One of Ordinary Skill in the Art Because They Address Different Problems**

One of ordinary skill would not combine the references to achieve the invention of claim 4 because the references are directed towards solving different problems. It is necessary to consider the reality of the circumstances--in other words, common sense--in deciding in which fields a person of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor. *In re Oetiker*, 977 F.2d 1443 (Fed. Cir. 1992); *In re Wood*, 599 F.2d 1032, 1036, 202 U.S.P.Q. 171, 174 (CCPA 1979). The cited references do not address the same problems.

In the case at hand, *Browen* is directed to solving the problem of testing for PCI-X protocol violations. For example, *Browen* provides that:

> An improved PCI-X verification method and apparatus provides iterative testing of all desired conditions or protocol combinations in a PCI-X system. One or more commands may be tested in combination with one or more functional behavior parameters throughout a desired range of variable parameter values. In one aspect, an apparatus and method for testing a PCI-X device for compliance under the PCI-X Addendum to the PCI Local Bus Specification in completer operation are provided. In another aspect, an apparatus and method for testing a PCI-X-device for compliance under the PCI-X addendum to the PCI Local Bus Specification in requester operation are provided.
>
> ...
>
> In one aspect, the present invention provides a method for the automatic testing of a PCI-X bus system in an information handling system, such as a computer system, comprising the steps of selecting a PCI-X command to be tested; programming a PCI-X requester to exhibit predetermined functional behavior during a PCI-X transaction; asserting the PCI-X command to initiate a PCI-X transaction, the transaction comprising transfer of data over the PCI-X bus; transferring at least a portion of the data; monitoring and recording the behavior of the PCI-X bus system; determining whether a PCI-X protocol error has occurred; if an error has occurred, logging the error and halting execution; repeating the process until it is determined that an error has occurred or until the PCI-X transaction is complete; and, if the PCI-X transaction is completed, writing data from a first memory location to a second memory location, reading data from the second memory location, and comparing data from the first memory location to data from the second memory location. In a further aspect, one or more commands may be tested in combination with one or more functional behavior parameters throughout a desired range of variable parameter values.

Browen, Abstract; col. 1, l. 53 - col. 2, l. 7.

On the other hand, *McCrory* is directed to the problem of modifying cache line requests in order to improve system performance. For example, *McCrory* provides as follows:

> [0004] Caching agents may request a read-only copy of a cache line or a read-write copy of a cache line. Some caching agents rarely write to the cache line, yet still request the cache line with read-write permission. When a caching agent requests a cache line with read-write permission, but does not write data to the

> cache line, many useless cache coherency operations may occur over the processor bus. For example, if an I/O device, such as a small computer system interface (SCSI) bus, or an Ethernet network interface card (NIC), requests a read-write copy of a cache line of data, the I/O device will receive the cache line with read-write permission and all other devices with a copy of that cache line will be forced to release their copy of the cache line. However, such an I/O device rarely writes to a cache line, rather, it typically sends the data to another device for viewing purposes. This creates useless cache coherency operations when caching agents are forced to release their copy of the cache line.
>
> [0005] Cache based computer systems lack explicit software controlled mechanisms that would enable software to modify cache line requests in order to improve overall system performance. Therefore, such a mechanism would be very desirable.

McCrory, p. 1, para. 0004, 0005.

Thus, the references address completely distinct problems that are unrelated to each other. Because the references address completely distinct problems, one of ordinary skill would have no reason to combine or otherwise modify the references to achieve the claimed invention. Thus, one of ordinary skill in the art would not combine these references as proposed by the Examiner. Accordingly, the Examiner has failed to state a prima facie obviousness rejection against claim 4.

For example, as shown above and below, when the technical details of the references are considered, the logical conclusion to draw is that one of ordinary skill would not combine the references because combining the references would provide no advantage in *Browen's* system. The reason for this fact is, in part, derived from the fact that the references address different problems. The Examiner has not overcome the specific deficiencies in *Browen* and *McCrory*, and has not overcome any of the specific facts pointed out by Applicants that show that one of ordinary skill would not combine the references when the references are considered as a whole. For this reason, and for the reasons already given, the Examiner has failed to state a prima facie obviousness rejection against claims 4 and 12.

V.A.v Summary of Why the Examiner Has Failed to State a Prima Facie Obviousness Rejection Against Claim 4

In general, the Examiner appears to proceed from the false assumption that just because individual elements of a claimed invention can be found in two or more references, combining the references would automatically render the claimed invention obvious to one of ordinary skill. In fact, the vast bulk of patentable inventions is derived from combinations of elements that can be found in the prior art.

In the case at hand, the Examiner has failed to state a prima facie obviousness rejection for the following reasons: The proposed combination does not teach all of the features of claim 4; no teaching, suggestion, or motivation exists to combine the references; the Examiner used impermissible hindsight

when fashioning the rejection; and the references would not be combined by one of ordinary skill in the art because they address different problems.

Therefore, Applicants respectfully urge that the rejections against claims 4 and 12 be withdrawn and that claims 4 and 12 be allowed.

V.B As to Claims 6-8, 14-16, 18, and 20

The Examiner has rejected claims 6-8, 14-16, 18, and 20 under 35 U.S.C. § 103(a) as being unpatentable over *Browen*, in view of *Ishida*, Method and system for generating image in computer graphics, United States Patent No. 6,456,283 B1 (Issued September 24, 2002) (hereinafter, "*Ishida*"). This rejection is respectfully traversed.

The Examiner has rejected claim 6 stating:

> Regarding **claim 6,** Browen teaches a method for transferring data from a memory to a network adapter (see col. 3, lines 6-7 and 12-13) . The reference teaches receiving a request (see Figure 3; col. 4, line 29) to transfer data in the memory to a network adapter; and setting a transfer size to align the data (see col. 4, lines 37-40; *"allows for full testing on various memory address alignments and cache boundaries")* with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size (see col. 4, lines 29-31) . Furthermore, Browen teaches transferring the amount of data in a frame, with a frame size (see col. 4, lines 45-47) .
> Although the Browen reference clearly teaches setting a length value according to the cache size, it does not specify whether the frame size is divisible by a cache line size with or without a remainder, in order to set the length, as claimed. Ishida teaches a method in which if the size is divisible with no remainder, a length is established equal to the length field. If it results in a remainder, it **sets the field to align** the data (see col. 8, lines 37-47) .
> At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a method of setting length fields applied to computer graphics, having "speedily" execution of functions, as taught by Ishida (see col. 1, lines 7-10) .

Office Action dated March 1, 2006, pp. 10-11.

Claim 6 is representative of all claims in this group and recites:

> 6. A method in a data processing system for transferring data from a memory to a network adapter, the method comprising:
> identifying frame size for a transfer of the data from the memory to the network adapter;
> setting a length equal to a cache line size;
> if the frame size is divisible by a cache line size without a remainder, setting a valid data length equal to the length field; and

if the frame size divided by the cache line size results in a remainder, setting the length field to align the data with the cache line size.

V.B.i The Proposed Combination Does Not Teach all of the Features of Claim 6

The Examiner has failed to state a *prima facie* obviousness rejection because the proposed combination does not teach all of the features of claim 6. In the case at hand, not all of the features of the claim have been considered and the teachings of the references themselves do not suggest the claimed subject matter to a person of ordinary skill in the art.

Claim 6 claims a method, and incorporates some features that are visually similar to, but distinct from some corresponding features of claim 1. The Examiner applies the same rationale to these features as the Examiner has applied against similarly situated features in claim 1. For example, claim 6 recites, "setting a length equal to a cache line size." Claim 1 recites, "setting a transfer size to align the data with a cache line size." The Examiner states vis-à-vis claim 1 feature,

> setting a transfer size to align the data (see col. 4, lines 37-40) with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size (see col. 4, lines 29-31).

Office action dated March 1, 2006, p. 6.

The Examiner states vis-à-vis claim 6 feature,

> setting a transfer size to align the data (see col. 4, lines 37-40) with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size (see col. 4, lines 29-31)

Office action dated March 1, 2006, p. 10.

The Examiner has not addressed the specific features of claim 6 in this rejection but instead copied the rejection of claim 1 verbatim. Notice should be taken that the features of claim 6 that the Examiner rejects are non-existent in claim 6. Claim 6 has no feature that recites "setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size." Therefore, the Examiner has failed to cite adequate teaching or suggestion of the specific features of claim 6 in the primary reference *Browen*. Therefore, whether *Ishida* provides support for the deficiencies that the Examiner concedes in *Browen* is immaterial. Therefore, the Examiner has failed to state a prima facie case of obviousness against claims 6-8, 14-16, 18, and 20 under 35 U.S.C. § 103(a).

Even if, *arguendo*, the Examiner had cited *Browen* as showing the feature "setting a length equal to a cache line size" of claim 6, such a rejection would be invalid as well. As Applicants have demonstrated in section IV above, *Browen* is devoid of any disclosure as to setting of any parameter equal

to a cache line size. Therefore, *Browen* cannot teach, "setting a length equal to a cache line size" as claimed.

Therefore, the combination of *Browen* in view of *Ishida* cannot teach all features of the claimed invention. Consequently, *Browen* in view of *Ishida* does not make claims 6-8, 14-16, 18, and 20 obvious under 35 USC § 103(a).

V.B.ii No Teaching or Suggestion Exists To Combine the References Because Each Reference Represents a Complete Solution to the Problem That Each Solves

Both *Browen* and *Ishida* represent complete solutions to the problems each solves. *Browen* shows a system for testing for PCI-X protocol violations. *Browen* represents a complete solution for fashioning such a system. On the other hand, *Ishida* shows a system for generating image in computer graphics while speedily executing hidden surface removal.

> It is an object to speedily generate a hidden surface removed image, by dividing one picture frame into a plurality of rectangular blocks and by repeating generation of a hidden surface removed block image.

Ishida, abstract.

Ishida represents a complete solution for fashioning such a system. Because each reference provides a complete solution to the problem that each reference represents, one of ordinary skill would have no reason to combine or otherwise modify the references. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against claims 6-8, 14-16, 18, and 20.

In addition, the Examiner has failed to state a *prima facie* obviousness rejection against features of claim 6, because the Examiner has not stated a proper teaching, suggestion, or motivation to combine the references. Instead, the Examiner has only stated a proposed advantage to combining the references. However, an advantage is not necessarily a teaching, suggestion, or motivation. To constitute a proper teaching, suggestion, or motivation, the Examiner must establish that one of ordinary skill would both recognize the advantage and have a reason to implement the advantage.

In the case at hand, the Examiner has not provided a sufficient reason why one of ordinary skill would recognize the proposed advantage or have a reason to implement it. The Examiner states,

> At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a method of setting length fields applied to computer graphics, having "speedily" execution of functions, as taught by Ishida (see col. 1, lines 7-10).

Office action dated March 1, 2006, p. 11.

However, the proposed motivation does not actually exist because *Browen* does not disclose setting a length field as Applicants have described in section IV above. Because *Browen* does not teach the feature "setting a length," such a feature cannot be borrowed from *Browen* and combined with *Ishida*.

If the proposed combination is not possible due to non-disclosure of the combined features in the references, the references cannot logically provide a motivation to combine the absent features either. For these reasons, the Examiner's statement fails to provide a proper teaching, suggestion, or motivation to combine the references. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against claims 6-8, 14-16, 18 and 20.

V.B.iii The Examiner Used Impermissible Hindsight When Fashioning the Rejection

In addition, the Examiner has failed to state a *prima facie* obviousness rejection against claim 6, because the Examiner used impermissible hindsight when fashioning the rejection. A simple substitution as the Examiner suggests would not add anything in *Ishida's* system that *Ishida's* system is not already able to do, and therefore will not produce the system as claimed by Applicants. *Ishida* fails to provide a reason to introduce frame size in *Browen's* system, and *Browen* fails to provide a reason why setting a length field in *Ishida* will be beneficial in the manner claimed by the Examiner, especially when *Browen* does not teach setting a length field for *Browen's* own use. Thus, none of the references teaches or suggests combining the references as posited by the Examiner, to achieve the results of the claimed method, and one of ordinary skill would have no reason to combine or otherwise modify the references.

Based on the plain disclosures in the references, the only suggestion to modify the references is found in Applicant's specification. Hence, the Examiner must have used Applicant's specification to find a teaching, suggestion, or motivation to combine the references. Doing so is impermissible hindsight and fails to comport with the standards of *Graham v. John Deere Co.*, 383 U.S. 1 (1966), which requires a proper teaching, suggestion, or motivation to combine or modify references to achieve a proper obviousness rejection. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against claims 6-8, 14-16, 18, and 20.

V.B.iv Summary of Why the Examiner Has Failed to State a Prima Facie Obviousness Rejection Against Claim 6

In general, the Examiner appears to proceed from the false assumption that just because individual elements of a claimed invention can be found in two or more references, combining the references would automatically render the claimed invention obvious to one of ordinary skill. In fact, that vast bulk of patentable inventions is derived from combinations of elements that can be found in the prior art.

In the case at hand, the Examiner has failed to state a prima facie obviousness rejection for the following reasons: The proposed combination does not teach all of the features of claim 6; no teaching or suggestion exists to combine the references because each reference represents a complete solution to the problem that each solves; and the Examiner used impermissible hindsight when fashioning the rejection.

Therefore, Applicants respectfully urge that the rejections against claims 6-8, 14-16, 18, and 20 be withdrawn and these claims be allowed.

VI Conclusion

Applicants respectfully urge that the subject application is patentable over *Holm*, *AAPA*, *Kennel*, and *Arndt*, and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: May 31, 2006

Respectfully submitted,

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APPENDIX A

Definition of the Absolute Value

The definition and properties of the **absolute value function** are explored interactively using an applet. The properties of basic **equations** and **inequalities** with **absolute value** are included.

For another tutorial on absolute value functions, go here.

Definition.

What is | x | ?

Click on the button above "click here to start" and maximize the window obtained. The point corresponding to x can be moved by dragging it.
On the left panel of the applet select "definition".
Two points are on the number line: a point corresponding to a real number a and a point corresponding to a real number x which can be dragged.
Use the slider on the left panel to set a to 0 (if it is not already). On the main panel (top left) are displayed x and | x |.
Now set x to 2, find the distance between the origin of the number line (0) and x. Compare this distance to | x | shown on the main panel.
Now set x to -2, find the distance between the origin of the number line (0) and x. Compare this distance to | x | shown on the main panel.
Repeat 3 and 4 above for x = 5 and x = -5 respectively.
What do you conclude when you compare the absolute values to the distances?
Check that (use other values for x if necessary)

$|x| = x$ when $x \geq 0$

and $|x| = -x$ when $x < 0$

What is | x - a | ?

Use the slider on the left panel to set a to 2 . On the main panel is displayed | x - a |.
Set x to 4, find the distance between the point corresponding to a and the point corresponding to x. Compare this distance to | x - a | shown on the main panel.
Set x to 0, find the distance between the point corresponding to a and the point corresponding to

x. Compare this distance to | x - a | shown on the main panel.
Repeat 3 and 4 above for x = 3 and x = 1 respectively.
What do you conclude when you compare the absolute values to the distances as defined above?
Check that (use other values for x and a if necessary)

| x - a | = x - a when x >= a

and

| x - a | = -(x - a) when x < a

Use the concept of distance to define | x - a |. (Note that | x | = | x - 0 |).

Use the Definition of the Absolute Value Function to Explore Basic Equations and Inequalities of the form:

| x - a | = b | x - a | < b | x - a | > b

On the left panel select "properties", set a (the top slider) to 0 and set b to 1 (the lower slider). The main panel (middle one) shows an equation

| x | = 1 (in dark green)

and two inequalities

| x | < 1 (in blue) and | x | > 1 (in red)

The solution of | x | = 1 is shown (dark green) as two points symmetric with respect to the origin: -1 and 1. Explain the two solutions.
The solution set to | x | < 1 is given by the blue interval (-1,1). Use the fact that | x | is a distance to explain the solution set.
The solution set to | x | > 1 is given by the union of the intervals (-infinity , -1) and (1,+infinity) (in red). Use the fact that | x | is a distance to explain the solution set.
Set a to 1 and b to 3. You now have the equation and inequalities

| x - 1 | = 3 | x - 1 | < 3 | x - 1 | > 3

Explain the two solutions of the equation and the solution sets of the two inequalities.
Use the results above and the definition to check that :

1 - $|x - a| = b$ is equivalent to: $x - a = b$ and $x - a = -b$

2 - $|x - a| < b$ is equivalent to: $-b < x - a < b$

3 - $|x - a| > b$ is equivalent to: $x - a > b$ or $x - a < -b$

Exercises: Answer the following questions analytically and use the applet to check the answers.

1 - Evaluate: a) $|-2|$ b) $|4|$

2 - Solve the equations: a) $|x| = 0$ b) $|x| = 3$ c) $|x - 2| = 1$

3 - Solve the inequalities: a) $|x| < 2$ b) $|x - 1| > 3$ c) $|x + 2| < 2$

Think about solving the following

a) $|x| = -2$

b) $|x - 4| < -4$

Source: http://www.analyzemath.com/Definition-Absolute-Value/Definition-Absolute-Value.html

APPENDIX B

WMLScript abs() Function

Back

The abs() function returns the absolute value of a number.

VI.A.i Syntax

```
n = lang.abs(x)
```

Part	Description
n	The absolute value returned from the function
x	The number to calculate the absolute value from

VI.A.ii Example

```
var a = lang.abs(-5);
var b = lang.abs(3.14);
```

VI.A.iii Result

```
a = 5
b = 3.14
```

Source: http://www.w3schools.com/wmlscript/lang_abs.asp